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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,538	11/07/2001	Luca Battu'	851763.420	2722

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EXAMINER	
PATEL, SHAMBHAVI K	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/008,538	BATTU' ET AL.	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Arguments/Amendment submitted 26 December 2006.

2. Claims 1-26 have been presented for examination. Claims 23-26 have been newly added.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Europe on 11/07/2000. The Examiner notes that a certified copy was submitted on 26 December 2006.

Response to Arguments

4. The Examiner notes that a certified copy of the foreign priority document was submitted on 26 December 2006.

5. Applicant's arguments filed 26 December 2006 regarding the 35 U.S.C. 101 rejection have been fully considered but they are not persuasive. Independent **claims 1 and 10** are directed to employing a hardware emulator for estimating the power consumption of a digital circuit. This claimed subject matter lacks a practical application of a judicial exception (law of nature, abstract idea, naturally occurring article/phenomenon) since it fails to produce a useful, concrete and tangible result. Specifically, the claimed subject matter does not produce a tangible result because the claimed subject matter fails to produce a result that is limited to having real world value rather than a result that may be interpreted to be abstract in nature as, for example, a thought, a computation, or manipulated data. More specifically, the claimed subject matter provides for estimating the power consumption. This produced result remains in the abstract and, thus, fails to achieve the required status of having real world value.

6. Applicant's arguments with respect to the art rejections of claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. **Claims 1-4, and 6-26 are rejected under 35 U.S.C. 101** because the claimed invention is directed to non-statutory subject matter. The Examiner asserts that the current state of the claim language is such that a reasonable interpretation of the claims would not result in any useful, concrete or tangible product. Independent **claims 1, 10 and 13** are directed to employing a hardware emulator for estimating the power consumption of a digital circuit. This claimed subject matter lacks a practical application of a judicial exception (law of nature, abstract idea, naturally occurring article/phenomenon) since it fails to produce a useful, concrete and tangible result. Specifically, the claimed subject matter does not produce a tangible result because the claimed subject matter fails to produce a result that is limited to having real world value rather than a result that may be interpreted to be abstract in nature as, for example, a thought, a computation, or manipulated data. More specifically, the claimed subject matter provides for estimating the power consumption. This produced result remains in the abstract and, thus, fails to achieve the required status of having real world value. All other claims are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

8. **Claim 1, 2, 4-7, 9, 10, 12, 13 and 15-26 are rejected under 35 U.S.C. 102(a)** as being clearly anticipated by **Weib ("Power Estimation Approach for SRAM-based FPGAs")**

Regarding claims 1, 10, and 13:

Weib discloses a process, system, and apparatus for estimating power consumption **(abstract and introduction)**, over a given time interval **(section 2.1 clock cycles)**, of a digital circuit described at a hardware level **(abstract)** using a functional element provided with input/output terminals **(sections 4.1 and 4.2)**, the process comprising estimating the power consumption based on the number of transitions performed by the functional element during said time interval **(section 2 equation 3 and section 2.1)** including

a. emulating at hardware level the digital circuit **(abstract)**, using additional elements associated to and coupled to said functional element at said hardware level **(sections 4.1 and 4.2)**, said additional element being able to detect at least one signal indicative of a behavior, and hence of power consumption of the associated functional element during said time interval **(sections 2-2.1)**.

b. acquiring a value of said at least one signal of the digital circuit, said value being indicative of the number of transitions and usable to determine the power consumption of said associated functional element is said given time interval **(sections 2-2.1 determining the toggle activity during a set number of clock cycles)**

Regarding claim 2:

Weib discloses coupling additional elements to an output of the functional element **(section 2)**. By coupling the emulator to the functional element **(sections 4.1-4.2)** the emulator can monitor the output pins to determine the toggle count.

Regarding claim 4:

Weib discloses controlling acquisition of the value of said at least one signal using hardware events monitored by logic analyzers active on the additional elements **(figure 3).**

Regarding claim 5:

Weib discloses the process according to claim 1, further comprising accessing information stored in said additional elements and storing said information in view of subsequent processing **(section 5).** The measurements are made during emulation and post-processing is performed in the form of evaluating the formulas.

Regarding claim 6:

Weib discloses a processing system configured to implement the process according to claim 1 **(figure 3).**

Regarding claim 7:

Weib discloses a computer program product directly loadable into an internal memory of a digital computer, comprising software code portions to perform the process of claim 1 when said program is run on the computer **(section 4).**

Regarding claims 9, 12, and 16:

Weib discloses the process of claim 1 wherein emulating at the hardware level includes emulating at a gate level **(section 3 6th-9th paragraphs).**

Regarding claim 15:

Weib discloses the apparatus of claim 13 wherein the third module includes machine-readable instructions stored on a machine-readable medium and executable by a processor **(section 4)**

Regarding claims 17, 20, and 22:

Weib discloses coupling said additional element to said functional element at said hardware level, wherein this modifies the digital circuit by forming part of said digital circuit at said hardware level, without modification of an original functionality of said digital circuit **(sections 2.1-2.4 and 4).** The toggle power mechanism works by associating itself with the output of the functional element. This is functionally equivalent to inserting itself into the hardware description, because by tying itself to the output pin, it can count the number of transitions on the signal.

Regarding claims 18, 19, 21, and 23:

Weib discloses using said additional elements to detect the number of transitions during operation of the digital circuit in real time **(section 4 1st paragraph).**

Regarding claims 24-26:

Weib discloses performing power estimation in cases than cannot be handled by software simulation **(section 3 6th paragraph).**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be

patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 3, 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weib ("Power Estimation Approach for SRAM-based FPGAs") in view of **Khouja (US Patent No. 6.075,932).**

Regarding claims 3, 11 and 14:

Weib discloses obtaining transition counts **(sections 2-2.1 determining the toggle activity during a set number of clock cycles).** Weib does not explicitly disclose calculating the percentage of time a signal is stable. **Khouja teaches** utilizing the static probability **(Khouja: column 7 lines 33-39)** to calculate the power consumption of a circuit. At the time of the invention, it would have been obvious to

combine the teachings of Weib and Khouja because the estimation of Khouja returns a power estimate in less cpu time than earlier approaches **(Khouja: column 7 lines 33-39)**

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Weib ("Power Estimation Approach for SRAM-based FPGAs") in view of **Raghunathan ("Register-Transfer Level Estimation Techniques for Switching Activity and Power Consumption").**

Regarding claim 8:

Weib does not explicitly disclose calculating the power consumption at RT level. **Raghunathan teaches** estimating the power consumption of a design at a register transfer level **(Raghunathan: title, abstract).** At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Weib and Raghunathan because estimating power consumption at the RTL is less time-consuming **(Raghunathan: Introduction).**

Conclusion

11. All claims are rejected.

12. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-22792279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

3/10/2007

Shambhavi Patel
Examiner
Art Unit 2128

KAMINI SHAH
SUPERVISORY PATENT EXAMINER